

Figure 1: Fail Map Circuit

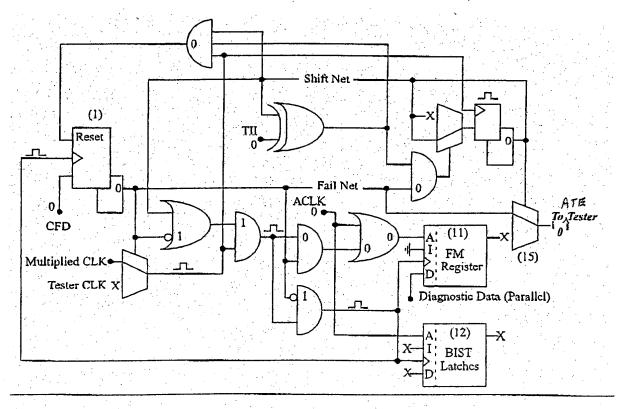


Figure 2: Fail Mapping before fail

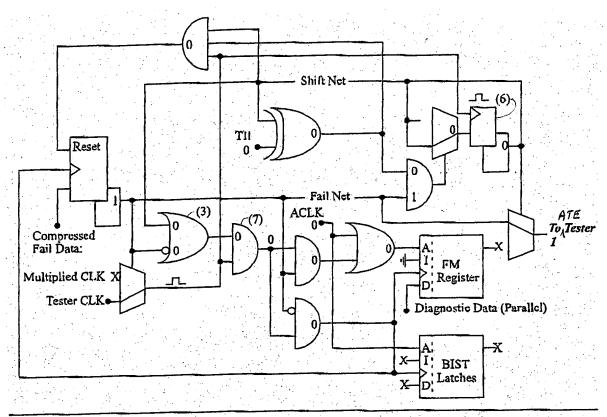


Figure 3: Fail Net asserted

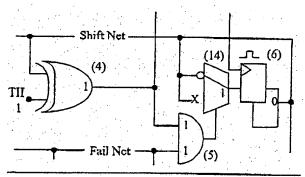


Figure 4: Asserting TII asserts Shift Net(+)

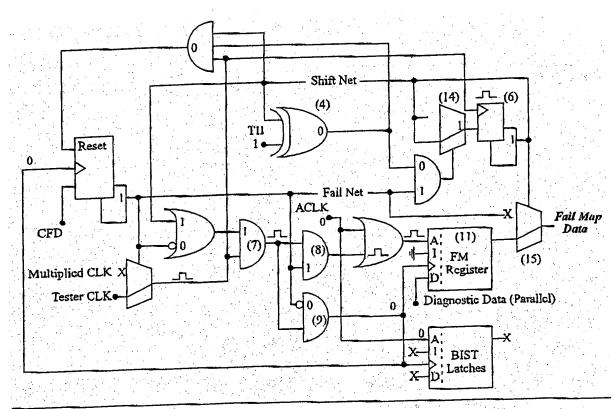


Figure 5: Fail Map Shift Out

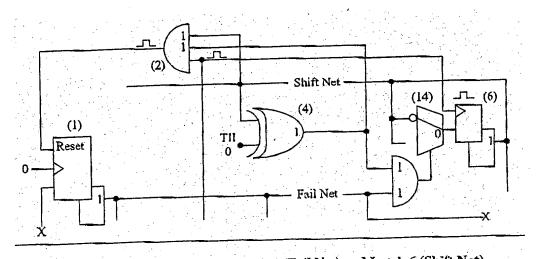


Figure 6: Clearing TII resets Latch 1 (Fail Net) and Latch 6 (Shift Net)

